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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/897,870	Applicant(s) SOMMER, RAINER	
	Examiner Kevin P Rizzuto	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2001, 01/16/2002, 07/04/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

2. Acknowledgement of papers filed: Application on 7/2/2001, foreign priority documents on 07/04/2001 and a new declaration on 1/16/2002. The papers filed have been placed on record.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. The certified copy of German Application 100 30 980.1, filed on 6/30/2000 has been received and placed on record.

Drawings

4. The drawings are objected to because they fail to have labels written directly on the drawings. Direct labeling using words and numbers, as opposed to only numbers, would enable the drawings to be read with greater ease. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining

figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Examiner recommends the following title: "Method for controlling the program run in a microcontroller based on information stored in another component or microcontroller."

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 3, 6, 7, 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. As per claim 3, applicant claims "at least one of an additional microcontroller, a control unit, and a control program executable on at least one microprocessor of the additional microcontroller." If a "control unit" is the "at least one" object that is used, then in line 6, the "controlling being performed as a function of information regarding a hardware of the additional microcontroller" would lack antecedent basis. It is not clear what applicant intended to claim and whether or not an additional microcontroller was optional or necessary.

9. As per claim 6,

-Applicant claims, "for testing at least one of a microcontroller, the control unit, and a program executable on at least one microprocessor of the microcontroller." Applicant later states, "storing another program," and later states, "the other program." It is unclear what "other program" refers to. If the "at least one" is a "control unit," then it is possible for no program to exist except the "another program" of line 4. In turn, it is unclear if "the other program" of line 5 always refers to the "another program" of line 4, or if applicant intended it to refer to a "program executable" of line 3.

-Applicant also claims, "a program executable on at least one microprocessor " and later states "another program executed on a computing element." Applicant also states in the specification that "a program that can be executed on a computing element, in particular on a microprocessor." It is unclear what distinguishes a microprocessor from a computing element and it is not described in the specification. It is recommended that "computing element" of claim 6 be replaced with "microprocessor."

10. As per claims 7, 8, and 9, each is dependent on 6 and therefore is also rejected under 35 U.S.C. 112, second paragraph.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1, 2, 3, 6, 7, 10, 11, 12, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Eckard et al., U.S. Patent 4,933,941.

13. As per claim 1, Eckard et al. disclose a method for controlling a run of a program (see below) executable on at least one microprocessor (auxiliary processor 21) of a microcontroller (items 21, 22, 23 and 105 of figure 2), comprising the steps of:

-The auxiliary processor 21 controls a test procedure sequence on another microprocessor (items 101, 102, 104 and 106) including the steps of loading of a test procedure sequence, initiating the test procedure sequence, and testing and comparing the results from the other microprocessor with the expected results stored in the microcontroller (items 21, 22, 23 and 105). A processor, a synonym for microprocessor, is defined as "a device that interprets and executes instructions, consisting of at least an instruction control unit and arithmetic unit." (The Authoritative

Dictionary of IEEE Standards Terms, 7th edition) For the auxiliary processor 21 to do these steps, by definition, it would be executing instructions, which together would constitute a program, and the program controls the testing of a device.

-Reading in information regarding a hardware (auxiliary processor 21) of the microcontroller from at least one information register (test mode register 23) of the microcontroller: (Figure 5, column 5, 44-61 and column 6, lines 12-16, 36-55; The test mode register 23 of figure 5 holds information about the microprocessor 21, including bit 10, which indicates processor 21 is in test enable mode and bits 0-3, which indicate when the test program should stop.)

-Actuating at least one switch via which the program run is controlled as a function of the information read in: (Figure 5, column 5, 44-61; The information register's information also includes stop and start switches (bits) that control the starting or stopping of the program. The switches are actuated at different times (i.e. going from a logic 1 to a 0, or a logic 0 to a 1), including when the program is to be stopped)

14. As per claim 2, the method according to claim 1, wherein:

-The information read in corresponds to at least one of the at least one microprocessors (auxiliary processor 21) of the microcontroller (items 21, 22, 23 and 105): (Column 5, lines 60-61; "Bit position 11 prevents the auxiliary processor 21 from stopping on a test procedure malfunction").

-And at least one additional component (auxiliary memory 22 and register array 105) of the microcontroller: (Column, lines 46-51; test mode register 23 contains information about whether or not to stop a program at a given memory address (of aux. Memory 22), a microaddress, or when a fault/error occurs. The fault/error is determined from information from the register array 105 as disclosed in column 5, lines 15-25).

15. As per claim 3, the method according to claim 1, further comprising the step of:

-Controlling a run of a test program that is executable on the at least one microprocessor (auxiliary processor 21) of the microcontroller (items 21, 22, 23 and 105) of a testing device (items 21, 22, 23, and 105): (Column 4, lines 64 to column 5, line 26; The auxiliary processor 21 controls a test procedure sequence on another microprocessor (items 101, 102, 104 and 106) including the steps of loading of a test procedure sequence, initiating the test procedure sequence, and testing and comparing the results from the other microprocessor with the expected results stored in the microcontroller (items 21, 22, 23 and 105) A processor, a synonym for microprocessor, is defined as "a device that interprets and executes instructions, consisting of at least an instruction control unit and arithmetic unit." (The Authoritative Dictionary of IEEE Standards Terms, 7th edition) For the auxiliary processor 21 to do these steps, by definition, it would be executing instructions, which together would constitute a program, and the

program controls the testing of a device, and therefore, it is a test program).

-And is for testing at least one of an additional microcontroller (items 101, 102, 103, 104 and 106), a control unit of the additional microcontroller (Instruction register 104), and a control program executable on at least one microprocessor of the additional microcontroller: (Column 5, lines 15-26 and Column 6, lines 35-55; the test program that is executed on auxiliary processor 21 tests the microprocessor (items 101, 102, 104 and 106) and its hardware (including cache memory unit 103). The additional microcontroller is made up of the execution unit 101, operand register array 102, cache memory unit 103, instruction register 104 and control apparatus 106 of figure 2. Each microcontroller has it's own memory, processor, registers and instructions which are shown in figure 2 and described throughout the specification)

- The instruction register 104 is a control unit because signals from the instruction register 104 are applied to the control apparatus 106 which controls the processing of the data signal groups as well as transfer signal groups between components (Column 1, lines 50-59). Column 5, lines 65-67; Eckard et al. teach that the test program tests "all of the apparatus in the central processing unit." Therefore, the testing device tests the control unit).

-The controlling being performed as a function of information regarding a hardware (cache memory unit 103) of the additional microcontroller (items

101, 102, 103, 104, 105 and 106): (Figure 5, column 5, 44-61 and column 6, lines 12-16, 36-55; The test mode register 23 of figure 5 holds information about fault/error bits regarding the cache memory unit 103. The auxiliary processor 21 controls the test program based on information within the test mode register 23, such as whether or not to stop the program from loading a different test procedure sequence after looking at the fault/error bits (column 5, lines 20-25)).

16. As per claim 6, Eckard et al. disclose a control element (item 21) for one of a control unit of an internal combustion engine and for a testing device (items 21, 22, 23 and 105) for testing at least one of a microcontroller (CPU 10), the control unit (instruction register 104), and a program executable (test procedure sequence) on at least one microprocessor (items 101, 102, 104, 106) of the microcontroller (CPU 10), comprising:

-The "internal combustion engine" of the preamble is given no patentable weight because it is intended use and no further mention or disclosure of it is given in the body of the claim.

-The instruction register 104 is a control unit because signals from the instruction register 104 are applied to the control apparatus 106 which controls the processing of the data signal groups as well as transfer signal groups between components (Column 1, lines 50-59). Column 5, lines 65-67; Eckard et al. teach that the test program tests "all of the apparatus in the central processing unit." Therefore, the testing device tests the control unit).

-A storage medium (auxiliary memory 22) storing another program that can be executed on a computing element (auxiliary processor 21): (The program is stored on Auxiliary Memory 22 of figure 2 and can be executed on a microprocessor (item 21) as is disclosed in column 4, lines 37-40)

-The other program causing the computer element to:

-Read in information regarding a hardware (cache memory unit 103) of the microcontroller (CPU 10) from at least one information register (test mode register 23) of the microcontroller (CPU 10): (Figure 5, columnn 5, 44-61 and column 6, lines 12-16, 36-55; The test mode register of figure 5 holds information about the central processing unit 10, including fault/error bits regarding the cache memory unit 103)

-Actuating at least one switch via which the program run is controlled as a function of the information read in: (Figure 5, column 5, 44-61; The information register's information also includes stop and start switches (bits) that control the starting or stopping of the program. The switches are actuated (i.e. going from a logic 1 to a 0, or a logic 0 to a 1) at different times, including when the program is to be stopped based on the information)

17. As per claim 7, Eckard et al. disclose the control element of claim 6, wherein:

-The computing element includes the at least one microprocessor: (Figure 2 teaches a computing element 10 that has an auxiliary processor 21).

18. As per claim 10, Eckard et al. disclose a microcontroller (items 21, 22, 23, 105), comprising:

-At least one microprocessor (auxiliary processor 21) including a program (see next bullet) that is executable on the at least one microprocessor: (Column 5, lines 3-10; the program is stored on Auxiliary Memory 22 of figure 2 and can be executed on central processing unit (CPU) 10)

- The auxiliary processor 21 controls a test procedure sequence on another microprocessor (items 101, 102, 104 and 106) including the steps of loading of a test procedure sequence, initiating the test procedure sequence, and testing and comparing the results from the other microprocessor with the expected results stored in the microcontroller (items 21, 22, 23 and 105). A processor, a synonym for microprocessor, is defined as "a device that interprets and executes instructions, consisting of at least an instruction control unit and arithmetic unit." (The Authoritative Dictionary of IEEE Standards Terms, 7th edition) For the auxiliary processor 21 to do these steps, by definition, it would be executing instructions, which together would constitute a program, and the program controls the testing of a device, and therefore, is a testing program)

-At least one information register: (Test mode register 23 of figure 2 is an information register and is described in column 5 lines 44-61.)

-An arrangement for reading in information regarding a hardware (auxiliary processor 21) of the microcontroller from the at least one information register: (Figure 5, column 5, 44-61 and column 6, lines 12-16, 36-55; The

test mode register 23 of figure 5 holds information about the microprocessor 21, including bit 10, which indicates processor 21 is in test enable mode and bits 0-3, which indicate when the test program should stop.)

- And at least one switch actuatable as a function of the information read in and for controlling a run of the program executable on the at least one microprocessor:: (Figure 5, column 5, 44-61; The information register's information also includes stop and start switches (bits) that control the starting or stopping of the program. The switches are actuated at different times (i.e. going from a logic 1 to a 0, or a logic 0 to a 1), including when the program is to be stopped)

19. As per claim 11, Eckard et al. disclose the microcontroller of claim 10 wherein:

-The information read in corresponds to at least one of the at least one microprocessors (auxiliary processor 21) of the microcontroller (items 21, 22, 23 and 105): (Column 5, lines 60-61; "Bit position 11 prevents the auxiliary processor 21 from stopping on a test procedure malfunction").

-And at least one additional component (auxiliary memory 22 and register array 105) of the microcontroller: (Column, lines 46-51; test mode register 23 contains information about whether or not to stop a program at a given memory address (of aux. Memory 22), a microaddress, or when a fault/error occurs. The fault/error is determined from information from the register array 105 as disclosed in column 5, lines 15-25).

20. As per claim 12, Eckard et al. disclose the microcontroller according to claim 11, wherein:

-The information regarding the at least one additional component of the microcontroller includes information about at least one of an internal storage element, an A/D converter, a D/A converter, and at least one databus: (The fault/error bits of test register 23 are determined from information from the register array 105 as disclosed in column 5, lines 15-25. Register array is a internal storage device).

21. As per claim 13, Eckard et al. disclose the microcontroller of claim 10, wherein:

-The microcontroller (items 21, 22, 23 and 105) is part of a testing device (items 21, 22, 23 and 105) for testing at least one of an additional microcontroller (items 101, 102, 103, 104 and 106 of figure 2), a control unit (items 103 and 104), and the program executable on the at least one microprocessor: (Column 5, lines 65-67; Eckard et al. teach that the test program tests "all of the apparatus in the central processing unit." Column 6, lines 36-42 disclose the testing of the cache memory unit. Cache memory unit 103 controls the instruction register 104 to cause one or more signal groups from the operand register 102 to be processed by the execution unit 101. It is also specifically stated that the cache memory is tested in column 6, lines 36-42. Signals from the instruction register 104 are applied to the control apparatus 106 which controls the processing of

the data signal groups as well as transfer signal groups between components (Column 1, lines 50-59).

22. As per claim 14, Eckard et al. disclose the microcontroller of claim 10 wherein:

-The microcontroller is part of a control unit for controlling/regulating technical operations and processes: (The microcontroller controls the testing of another microcontroller, which is done by execution of programs that are technical operations and processes. Technical is defined as "Having special skill or practical knowledge especially in a mechanical or scientific field" (The American Heritage College Dictionary). Process is defined as "A series of actions, changes, or functions bringing about a result "(The American Heritage College Dictionary). Therefore, an execution of a program is a process because it's a series of instructions that produce a result and it is a technical operation because in order to have instructions capable of executing a program, especially a debugging program, some special skill is required.

23. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Chesters et al., U.S. Patent 6,175,913.

24. As per claim 1, Chesters et al. disclose a method for controlling a run of a program executable on at least one microprocessor (item 7, figure 1) of a microcontroller (item 1, figure 1), comprising the steps of:

-Reading in information regarding a hardware of the microcontroller from at least one information register of the microcontroller: (Figure 2, items 15,

15a, 16, 17, 17a, and 18 and column 3 lines 15-32. The items 15, 15a, 16, 17, 17a, and 18 are all registers that contain information about the memory, including protection information and availability information.)

-Actuating at least one switch via which the program run is controlled as a function of the information read in: (Column 3, lines 15-34; the information also actuates multiple control switches (i.e. setting bits from a logic 0 to a 1 or a logic 1 to a 0) and are actuated on certain conditions if data or code is accessed or executed. For example, the execute signal bit (switch) in code range entries enables single stepping of instructions within the associated range (program control)).

25. As per claim 4, Chesters et al. disclose the method according to claim 1, further comprising the step of:

-Controlling a run of a control program that is executable on the at least one microprocessor of the microcontroller of a control unit: (Figure 1 item 7 shows the CPU that programs are executed on. Column 3, lines 15-34 disclose an execute signal bit in code range entries that enables single stepping of instructions within the associated range (program control)).

-And is for controlling/regulating technical operations and processes: (The registers control the execution of programs that are technical operations and processes. Technical is defined as "Having special skill or practical knowledge especially in a mechanical or scientific field" (The American Heritage College Dictionary). Process is defined as "A series of actions, changes, or functions bringing about a result "(The American Heritage

College Dictionary). Therefore, an execution of a program is a process because it's a series of instructions that produce a result and it is a technical operation because in order to have instructions capable of executing a program, especially a debugging program, some special skill is required.

-The controlling being performed as a function of the information regarding the hardware of the microcontroller: (Figure 2, items 15, 15a, 16, 17, 17a, and 18 and column 3 lines 15-32. The items 15, 15a, 16, 17, 17a, and 18 are all registers that contain information about the memory, including protection information and availability information. The mode registers 15a and 17a contain bits which indicate whether a read, a write, or an execute in the specified range will be allowed, which is controlling how a program can execute.)

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chesters et al. in view of Simar Jr. et al., U.S. Patent 6,182,203.

28. Chesters et al. disclose the method as applied to claims 1 and 4, but fail to specifically teach that the technical operations and processes relate to a motor vehicle.

29. Simar Jr. et al. teaches the use of processors in engine control units for motor vehicles in Figure 83 and column 88, lines 36-59.

30. Chesters et al. teach a processor for application in critical real-time systems as show in column 1, lines 37-44. Simar Jr. et al. also teach a processor for real-time applications as shown in column 2, lines 28-33. Simar Jr. et al. also specifically teach the use of their processor for real-time applications being used in engine control in column 88, lines 36-59. Therefore, it would have been obvious to one of ordinary skill in the art to use the disclosed processor of Chesters et al. in a vehicle because it is qualified for real-time applications such as for use in an engine.

31. The reasons stated above would have provided the motivation to use Chesters et al. invention for technical operations and processes relating to a motor vehicle.

32. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eckard et al. in view of IEEE Dictionary.

33. As per claim 8, Eckard et al. disclose the control element as applied to claim 6 above, but fails to specifically teach the memory to be flash memory and read only memory.

34. IEEE dictionary states the read-only memory (ROM) is "A type of permanent data storage (memory) that can be read but not altered by the

system. Data stored in read-only memory is not affected by power loss to the system."

35. It would have been obvious to someone of ordinary skill in the art to specifically choose ROM because of the advantages associated with it as described in the definition above. Users cannot alter it once it has been manufactured, which will prevent tampering. It also is not affected by power loss, which would be desired in a system that would be applied to a vehicle.

36. One of ordinary skill in the art would have been motivated to specifically choose ROM for type of memory for the above-mentioned advantages.

37. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eckard et al. in view of Simar Jr. et al., U.S. Patent 6,182,203.

38. Eckard et al. disclose the control unit as applied to claim 6 and the microcontroller of claim 10, but fail to specifically teach that the control element is one for a control unit of an internal combustion engine of a motor vehicle.

39. Simar Jr. et al. teaches the use of processors in engine control units for motor vehicles in Figure 83 and column 88, lines 36-59.

40. Eckard et al. teach an apparatus for testing the operation of a typical CPU, which has a complexity that provides an enormous opportunity for malfunction in column 2, lines 20-21. Eckard et al. also teach that the apparatus has a minimum impact on performance in column 3, lines 29-34. Simar Jr. et al. disclose the processor for use in real-time applications in column 2, lines 28-33. It is well known in the art that real-time applications require minimum impacts on performance. It would have been obvious to one of ordinary skill in the art that a

CPU that is as complex as the one disclosed in Simar Jr. et al. would have an enormous opportunity for malfunction. Simar Jr. et al. also disclosed its need for real-time applications, which would require a minimum impact on performance when testing the CPU. Therefore, it would have been obvious to one of ordinary skill in the art to use Eckard et al.'s disclosed invention with the CPU of Simar Jr. et al..

41. The need for testing the CPU of Simar Jr. et al. with a minimum impact on performance would have provided the motivation to use the Eckard et al. invention for technical operations and processes relating to a motor vehicle.

Conclusion

42. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (703)305-6783. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

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